



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/519,394

12/22/2004

Christoph Siegelin

76.0733/PR

2863

41754 7590 02/02/2009
THE JANSSON FIRM
9501 N. CAPITAL OF TX HWY #202
AUSTIN, TX 78759

EXAMINER

CHRZANOWSKI, MATTHEW R

ART UNIT

PAPER NUMBER

2186

MAIL DATE

DELIVERY MODE

02/02/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/519,394	Applicant(s) SIEGELIN ET AL.	
	Examiner MATTHEW R. CHRZANOWSKI	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 13, 23-31, 38-39, and 41 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Consider **claim 13**, as claimed, is merely drawn to nonstatutory descriptive material since the claim is of a “computer program”. Giving the claim a reasonable interpretation, the claim is of software or computer program code only, and does not impart any functionality as being employed as a hardware component, since the it is not claiming a physical computer readable medium which comprises software which when executed by a processor causes the processor to produce a useful, concrete, and tangible result. Software or program code is non-statutory subject matter and not patentable. Dependent **claims 23-31, 38-39, and 41** inherit this defect.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 11, 12, 40, and 41** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claim limitation of claims 11 and 12 “designated as an active physical area and if the new programming operation requires an erase operation to the active physical areas, designating the active area to be an unwritten physical area in the mirror memory” is not set forth in the specification, and is considered new matter. The claim limitation of claims 40 and 41 “in response to determining that writing to the active physical area would require an erase operation, designating an unwritten physical area in the mirror area as the active physical area” is not set forth in the specification, and is considered new matter. Additionally the specification does not recite "unwritten physical area" nor define such a term.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2186

5. **Claims 1-2, 11, 13, 23, 32-35, 38-41** rejected under 35 U.S.C. 102(b) as being anticipated by **Ban (WO 94/20906 hereinafter “Ban”)**.

Consider **claims 1 and 13**, Ban discloses a method to write in flash type memory (*flash memory, abstract; method (i.e., software, or firmware of hardware)...*, page 2, lines 7-10) of an electronic module comprising:

defining a mirror area in the flash type memory (*block, areas, units, or zones: page 2, line 21-page 3, line 15, page 3, lines 1-2*) divided into at least two physical areas (*flash memory physical address locations, page 2, line 21*) each designated to correspond to a same logical area for storing content written to the logical area (*fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of unique Logical areas associated with a fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2, line 21-page 3, line 15*);

designating one of the physical areas as being an active physical area; and during a write (*abstract*) to said logical area, programming the content of said logical area into the active area (*flash memory system which “allows data to be continuously written to unwritten physical address locations,” abstract; data cannot be*

written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).

Consider **claims 2 and 23**, and as applied to **claims 1 and 13** above, Ban discloses the method further comprising erasing the content of all physical areas in a memory area in a single operation at a convenient time (*"One or more physically contiguous flash memory areas (called zones) that can be physically erased using suitable prior art flash memory technology comprise a unit and each unit contains an integral number of blocks,"* page 3, lines 4-7; there is a zone erase operation that erases the unit that includes that block, and unit containing the logical block consisting of multiple physical address locations are therefore all erased, the page 3, lines 24-25) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).

Consider **claim 11**, Ban discloses an electronic module comprising information processing means (*the device writes and stores data, abstract*) and comprising a flash type non volatile memory (*flash memory, abstract*) having a mirror memory formed from at least two physical areas (*flash memory physical address locations, page 2, line 21*) each

designated to correspond to contain a same logical area (*fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of unique Logical areas associated with a fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2, line 21-page 3, line 15*), each new programming operation in said logical area taking place in one of the physical areas of the mirror memory (*flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29*) (*page 7, lines 1 - page 9, line 22 and page 13, claim 1*) designated as an active physical area and if the new programming operation requires an erase operation to the active physical areas, designating the active area to be an unwritten physical area in the mirror memory (*data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29 and page 4, lines 10-17; page 7, lines 1 - page 9, line 22 and page 13, claim 1*).

Consider **claim 32 and 38**, and as applied to **claim 1 and 13**

above, Ban discloses the method wherein each physical area has a status which is one of three statuses (*each block denotes its status: page 7, lines 11-14; each block maps to physical address, therefore each physical area has a status: FIG. 4*): blank (*block free and writable: page 7, line 13*), active (*block allocates and contains user data: page 7, line 13-14*) and used (*block deleted and not writable: page 7, line 13*).

Consider **claim 33 and 39**, and as applied to **claim 32 and 38**

above, Ban discloses the method wherein:

the blank status corresponds to one of the physical areas ready to receive data but not selected for receiving data (*block free and writable: page 7, line 13*),

the active status corresponds to one of the physical areas ready to receive data and selected for receiving data or to one of the physical areas containing the actual content of the logical area to be read (*block allocates and contains user data: page 7, line 13*),

the used status corresponds to one of the physical areas containing an outdated data that shall not be read, said physical area waiting for an erasure (*block deleted and not writable: page 7, line 13*).

Consider **claim 34**, and as applied to **claim 11** above, Ban discloses the method wherein each physical area has a status which is one of three statuses (*each block denotes its status: page 7, lines 11-14; each block maps to physical address, therefore each physical area has a status: FIG. 4*): blank (*block free and writable: page 7, line 13*), active (*block allocates and contains user data: page 7, line 13-14*) and used (*block deleted and not writable: page 7, line 13*).

Consider **claim 35**, and as applied to **claim 34** above, Ban discloses the method wherein:

the blank status corresponds to one of the physical areas ready to receive data but not selected for receiving data (*block free and writable: page 7, line 13*),

the active status corresponds to one of the physical areas ready to receive data and selected for receiving data or to one of the physical areas containing the actual content of the logical area to be read (*block allocates and contains user data: page 7, line 13*),

the used status corresponds to one of the physical areas containing an outdated data that shall not be read, said physical area waiting for an erasure (*block deleted and not writable: page 7, line 13*).

Consider **claims 40 and 41**, and as applied to **claims 1 and 13** above, Ban discloses the method wherein the method further comprises:

determining whether writing to the active physical area would require an erase operation prior to writing; in response to determining that writing to the active physical area would require an erase operation, designating an unwritten physical area in the mirror area as the active physical area; and storing an indication that the active physical area is a written memory area (*data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29 and page 4, lines 10-17; page 7, lines 1 - page 9, line 22 and page 13, claim 1; page 3, lines 19-24*).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

Art Unit: 2186

said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 3, 7-8, 18, 24, and 28-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** as applied to **claims 1-2, 13, and 23** above, and further in view of **Assar et al. (WO 95/10083 hereinafter “Assar”)**.

Consider **claims 3 and 24**, and as applied to **claims 2 and 23** above, Ban discloses the method wherein there is a convenient time as described above in claim 2 and 23.

However, Ban does not disclose the method comprising performing the erasure during a period of inactivity or when all the physical areas are used.

Assar discloses a method comprising performing an erasure when all the physical areas are used (*when physical memory is filled, blocks*

with certain flags set are erased, wherein as described above blocks contain multiple physical mirror areas, page 20, lines 10-19).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform an erasure when all the physical areas are used in the system of Ban, because Assar teaches it is necessary to erase some data when a memory is full in order to place new data in a flash memory (*page 20, lines 10-19*).

Consider **claims 7 and 28**, and as applied to **claims 1 and 13** above, Ban discloses the method comprising designating said active physical areas (*active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1*).

However, Ban does not disclose the method comprising designating said active physical areas using a counter and incrementing the counter on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter (*counter 620 page 18, lines 26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112*) and incrementing the counter on each change of active area (*page 20, lines 10-19*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical

areas using a counter in the system of Ban, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next (*page 18, lines 26-28; abstract*).

Consider **claims 8 and 29**, and as applied to **claims 1, 13, 23 and 24** above, Ban discloses the method of claims 1 and 13.

However, Ban does not disclose the method comprising associating at least one bit with a logical area to represent the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit (*one bit used flag 626, page 18, line 36*) with a logical area (*data block, page 18, lines 31-37*) to represent the use state of at least one physical area of said logical area (*page 18, lines 35-37*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area to represent the use state of at least one physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle (*page 7, lines 9-21*).

Consider **claim 18**, and as applied to **claim 7** above, Ban in view of Assar discloses the method of claim 7.

However, Ban does not disclose the method comprising associating at least one bit with a logical area representing the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit (*one bit used flag 626, page 18, line 36*) with a logical area (*data block, page 18, lines 31-37*) representing the use state of at least one physical area of said logical area (*page 18, lines 35-37*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area representing the use state of at least one physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle (*page 7, lines 9-21*).

9. **Claims 4 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** as applied to **claims 1 and 13** above, and further in view of **Mennecart (WO 01/88926 A1 hereinafter “Mennecart”)**.

Consider **claims 4 and 25**, and as applied to **claims 1 and 13** above, Ban discloses the method of claims 1 and 13.

However Ban does not disclose the method comprising copying the active physical area into a buffer area, erasing all physical areas and copying the buffer into a first available physical area in the mirror area.

Mennecart discloses method comprising copying the active physical area into a buffer area (*buffer, abstract; step F5, temporary storage, FIG. 4*), erasing all physical areas (*steps F3 and F3', FIG. 4*) and copying the buffer into a first available physical area (*page 5, line 1 – page 6, line 22; step F7, FIG. 4*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to copy the active physical area into a buffer area, erase all physical areas and copy the buffer into a first area available in the system of Ban, because Mennecart teaches the method to process a write command in memory such as EEPROM, a type of flash memory in smart cards, which reduces the time required for processing (*page 3, lines 9-35; abstract*).

10. **Claims 5 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** as applied to claim **claims 2 and 23** above, and further in view of **Hazen et al. (WO 99/35650 hereinafter “Hazen”)**.

Consider **claims 5 and 26**, and as applied to **claims 2 and 23** above, Ban discloses the method comprising performing an erasure as described in claims 2 and 23.

However, Ban does not disclose the method comprising the erasure and programming/read operations in parallel thereby not blocking the electronic module.

Hazen discloses a method comprising programming/read operations in parallel thereby not blocking an electronic module (*"read-while-write operations," title; abstract; page 2, paragraph 4; pages 5-7*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel with erasure thereby blocking an electronic module in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in terms of time constraints (*page 2, paragraph 2 and page 3, paragraph 1*).

11. **Claims 6 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claims 5 and 26** above, and in view of **Lipovski (US Patent # 5758148)**.

Consider **claims 6 and 27**, and as applied to **claims 5 and 26** above, Ban in view of Hazen discloses the method wherein comprises performing the erasure and programming/read operations in parallel, having mirror memory area(s), one area being used for programming/reading while the other area is erased as described above in claims 5 and 26.

However, Ban does not disclose the method wherein comprises performing the erasure and programming/read operations in parallel **in a bi-bank memory**, said bi-bank memory corresponding to the mirror memory area each bank having mirror area(s), one bank being used for programming/reading while the other bank is erased, **changing active bank when all physical areas of the bank used for programming/read have been used**.

Hazen discloses the method wherein comprises performing the erasure and programming/read operations in parallel (*one device may be written to, while the other device is being erased, page 2, paragraph 3*) in a bi-bank memory (*multiple flash memory devices, page 2, paragraph 3*), said bi-bank memory corresponding to the mirror memory area (*Ban teaches mirror memory areas in memory, while Hazen teaches bi-bank memory as a type of memory*) each bank having physical area(s) (*as described in claims 5 and 26*), one bank being used for programming/reading while the other bank is erased (*one device may be written to, while the other device is being erased, page 2, paragraph 3*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel in a bi-bank memory in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in term of time constraints (*page 2, paragraph 2; and page 3, paragraph 1*).

Lipovski discloses a method of changing an active bank when all physical areas of the bank used for programming/read have been used (*one memory bank reaches its capacity, the system switches to the other bank to permit data writes, column 11, lines 38-42*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to change the active bank when all areas of the active bank have been used for programming operations in the system of Ban, because Lipovski teaches this allows to continue writing to memory without erasing the full memory bank (*column 11, lines 38-42*).

12. **Claims 9-10 and 30-31** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** as applied to **claims 1-2 and 13** above, and further in view of **Kuo (US Patent # 4763305 hereinafter “Kuo”)**.

Consider **claims 9 and 30**, and as applied to **claims 1 and 13** above, Ban discloses wherein the write is carried out as claims 1 and 13 above.

However, Ban does not disclose the method, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area in the mirror area otherwise.

Kuo discloses a method, wherein if the content of the logical area is identical to the content of the active physical area, a write is carried out in an active physical area (*if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26*), and in a blank physical area otherwise (*if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase (*column 6, lines 29-30*).

Consider **claims 10 and 31**, and as applied to **claims 9 and 30** above, Ban discloses the method comprising programming (*writing*) of the logical area in the blank physical area in claim 1 and 13.

However, Ban does not disclose the method comprising programming only a portion of the logical area in the blank physical area.

Kuo discloses a method comprising programming only part of the logical area in the blank physical area (*only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only part of the logical area in the blank physical area in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase (*column 6, lines 29-30*).

13. **Claim 12, 36, and 37** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** and further in view of **Robinson et al. (US Patent # 5375222)**.

Consider **claim 12**, Ban discloses an electronic module having information processing means (*the device writes and stores data,*

abstract) and a flash type non volatile memory (*flash memory, abstract*) having a mirror memory formed from at least two physical areas (*flash memory physical address locations, page 2, line 21*) each designated to correspond to a same logical area (*fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of unique Logical areas associated with a fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2, line 21-page 3, line 15*), each new programming operation to said logical area taking place in one of the physical areas of the mirror memory (*flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29*) (*page 7, lines 1 - page 9, line 22 and page 13, claim 1*) designated as an active physical area and if the new programming operation requires an erase operation to the active physical areas, designating the active area to be an unwritten physical area in the mirror memory (*data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29*

and page 4, lines 10-17; page 7, lines 1 - page 9, line 22 and page 13, claim 1).

However, Ban does not disclose the flash memory module being on a card.

Robinson discloses a card comprising an electronic module having information process means and a flash type non volatile memory (*abstract; title*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a card in the system of Ban, because Robinson teaches it as a way of encasing flash memory and logic circuitry to perform operations of storing and outputting data (*abstract*).

Consider **claim 36**, and as applied to **claim 12** above, Ban in view of Robinson discloses the method wherein each physical area has a status which is one of three statuses (*Ban: each block denotes its status: page 7, lines 11-14; each block maps to physical address, therefore each physical area has a status: FIG. 4*): blank (*Ban: block free and writable: page 7, line 13*), active (*Ban: block allocates and contains user data: page 7, line 13-14*) and used (*Ban: block deleted and not writable: page 7, line 13*).

Consider **claim 37**, and as applied to **claim 36** above, Ban in view of Robinson discloses the method wherein:

the blank status corresponds to one of the physical areas ready to receive data but not selected for receiving data (*Ban: block free and writable: page 7, line 13*),

the active status corresponds to one of the physical areas ready to receive data and selected for receiving data or to one of the physical areas containing the actual content of the logical area to be read (*Ban: block allocates and contains user data: page 7, line 13*),

the used status corresponds to one of the physical areas containing an outdated data that shall not be read, said physical area waiting for an erasure (*Ban: block deleted and not writable: page 7, line 13*).

14. **Claims 14-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** in view of **Hazen et al. (WO 99/35650 hereinafter “Hazen”)** as applied to **claims 5 and 6** above, and further in view of **Assar et al. (WO 95/10083 hereinafter “Assar”)**.

Consider **claims 14 and 15**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method comprising designating

said active physical areas (*active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1*).

However, Ban in view of Hazen does not disclose the method comprising designating said active physical areas using a counter and incrementing the counter on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter (*counter 620 page 18, lines 26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112 and incrementing the counter on each change of active area (page 20, lines 10-19)*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a counter in the system of Ban in view of Hazen, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next (*page 18, lines 26-28; abstract*).

Consider **claims 16 and 17**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method of claims 5 and 6.

However, Ban in view of Hazen does not disclose the method comprising associating at least one bit with a logical area to represent the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit (*one bit used flag 626, page 18, line 36*) with a logical area (*data block, page 18, lines 31-37*) to represent the use state of at least one physical area of said logical area (*page 18, lines 35-37*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area to represent the use state of at least one physical area of said logical area in the system of Ban in view of Hazen, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle (*page 7, lines 9-21*).

15. **Claims 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** in view of **Hazen et al. (WO 99/35650 hereinafter “Hazen”)** as applied to **claims 5 and 6** above, and further in view of **Kuo (US Patent # 4763305 hereinafter “Kuo”)**.

Consider **claims 19 and 20**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses wherein the write is carried out as claims 5 and 6 above.

However, Ban in view of Hazen does not disclose the method, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

16. **Claim 21-22** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter “Ban”)** in view of **Assar et al. (WO 95/10083 hereinafter “Assar”)** as applied to **claim 7** above, and further in view of **Kuo (US Patent # 4763305 hereinafter “Kuo”)**.

Consider **claim 21**, and as applied to **claim 7** above, Ban in view of Assar discloses wherein the write is carried out as claim 7 above.

However, Ban in view of Assar does not disclose the method, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Assar, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Consider **claim 22**, and as applied to **claim 21** above, Ban in view of Hazen and Kuo discloses the method comprising programming (*writing*) of the logical area in the blank physical area in claim 1.

However, Ban in view of Hazen does not disclose the method comprising programming only a portion of the logical area in the blank physical area.

Kuo discloses a method comprising programming only a portion of the logical area in the blank physical area (*only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only a portion of the logical area in the blank physical area in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase (*column 6, lines 29-30*).

Response to Arguments

17. Applicant's arguments filed 01/09/2009 have been fully considered but they are not persuasive. See above revised rejections and further explanation below.

35 USC 102

Claim 1

Art Unit: 2186

18. Applicant argues Ban does not teach the steps of "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" (*remarks, pages 13-18*) and "One of the areas is "designat[ed] ... as being an active physical area", and "during a write to said logical area, programming the content of said logical are into the active physical area" (*remarks, pages 13-18*). Examiner respectfully disagrees. As stated above in the revised rejections, Ban discloses the limitations. See recited rejection below for convenience:

defining a mirror area in the flash type memory (*block, areas, units, or zones: page 2, line 21-page 3, line 15, page 3, lines 1-2*) divided into at least two physical areas (*flash memory physical address locations, page 2, line 21*) each designated to correspond to a same logical area for storing content written to the logical area (*fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of unique Logical areas associated with a fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2, line 21-page 3, line 15*);

Art Unit: 2186

designating one of the physical areas as being an active physical area; and during a write (*abstract*) to said logical area, programming the content of said logical area into the active area (*flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

19. Ban discloses two physical areas (physical byte addresses) each designated to correspond to a same logical area (zone and logical block) for storing content written to the logical area (*page 3, lines 1-7*). Applicant appears to reading into the claim language (*Remarks pages 12-18*) that Ban's "logical block" must correspond to Applicant's "logical area". However, the claim language does not recite or imply this mapping.

20. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a stationary association of a group of physical areas to a same and unique logical area, and arguments concerning Figures on pages 14 and 15 of Remarks) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Art Unit: 2186

21. Applicant argues Ban teaches a one-to-one mapping (pages 16-18 of Remarks). However, as evidenced above, and Ban discloses two physical areas (physical byte addresses) each designated to correspond to a same logical area (zone and logical block) for storing content written to the logical area (*page 3, lines 1-7*). Therefore, a single logical block contains a fixed-length group (plurality of) of physical byte addresses. This mapping is clearly not one-to-one.

Claims 11 and 13

22. Applicant argues claims 11 and 13 for the same reasons as claim 1. Examiner respectfully disagrees. See above response to arguments and claim rejections concerning the claims in question.

Claims 2, 23, 32-35 and 38-39

23. Applicant argues the dependent claims are allowable due to their dependence upon the independent claims. Examiner respectfully disagrees. See above response to arguments and claim rejections concerning the claims in question.

24. Applicant argues claims 2, 23, 32-35 and 38-39 provide further unique and non-obvious combinations. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

35 USC 103

25. Applicant argues the claims are allowable for the same reasons with respect to claims 1, 11, 12 and 13 rejected under 35 USC 102 over Ban. Examiner respectfully disagrees. See above response to arguments and claim rejections concerning the claims in question.

26. Applicant argues the added references under 35 USC 103 do not teach the amended claim language of claim 1, and analogous in the other independent claims as well, For the same reasons above. See above response to arguments and claim rejections concerning the claims in question.

27. Applicant argues the dependent claims are allowable due to their dependence upon the independent claims. Examiner respectfully disagrees. See above response to arguments and claim rejections concerning the claims in question.

28. Applicant argues dependent claims provide further unique and non-obvious combinations. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

29. Applicant argues claims 9, 30 and 40, for the same reasons as claim 1 (*Because Ban does not teach or suggest "defining a mirror area in the flash memory type divided into at least two physical areas...it is not surprising that Ban does not teach allocating a blank physical area in the mirror area" page 20 of*

Art Unit: 2186

Remarks). Examiner respectfully disagrees. See above response to arguments and claim rejections concerning the claims in question.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW R. CHRZANOWSKI whose telephone number is (571)270-1176. The examiner can normally be reached on M-F 9am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Matthew R Chrzanowski
Examiner
Art Unit 2186

/M. R. C./
Examiner, Art Unit 2186
2/2/2009